N-Channel and P-Channel Complementary MOSFET

Product Summary

NMOS

V_{DS}	100V
I_D	5A
$R_{DS(ON)}$(at V_{GS}=10V)	27m
$R_{DS(ON)}$(at V_{GS}=4.5V)	30m

PMOS

V_{DS}	-100V
I_D	-3A
$R_{DS(ON)}$(at V_{GS}=-10V)	110m
$R_{DS(ON)}$(at V_{GS}=-4.5V)	120m

General Description

Trench Power LV MOSFET technology

Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

ptible power supply

Absolute Maximum Ratings (T_A=25 unless otherwise noted)

NMOS Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	
		V_{DS}=100V, V_{GS}=0V, Tj=150	-	-	100	

PMOS Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V, V_{GS}=0V	-	-	-1	
		V_{DS}=-100V, V_{GS}=0V, Tj=150	-	-	-100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ± 20V, V_{DS}=0V	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250	-1	-1.7	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-3A	-	85	110	m
		V_{GS}=				

NMOS Typical Electrical and Thermal Characteristics Diagrams

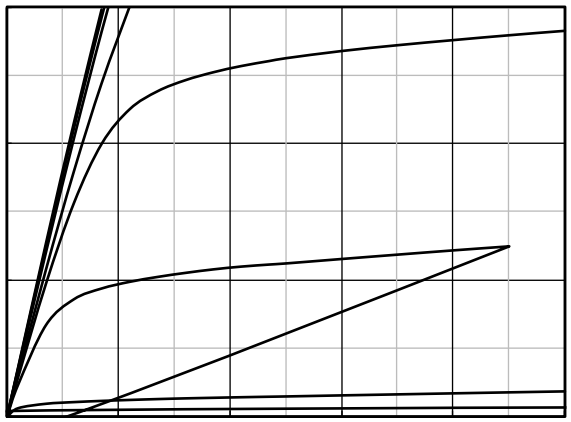


Figure 1. Output Characteristics

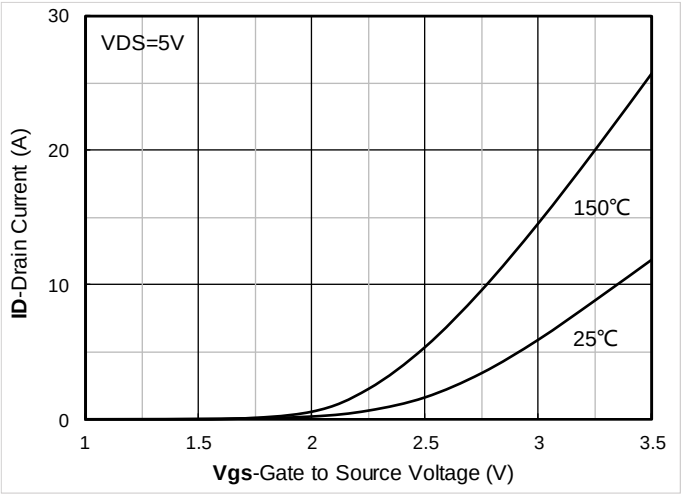


Figure 2. Transfer Characteristics

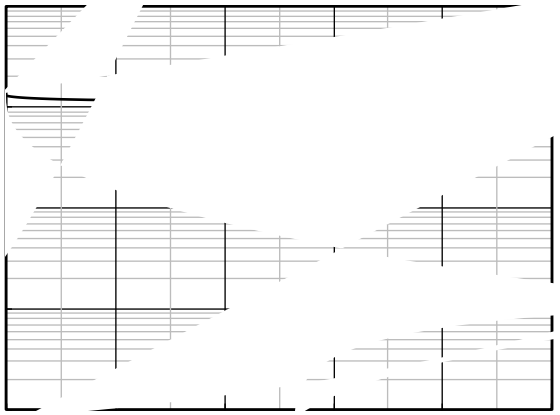


Figure 3. Capacitance Characteristics

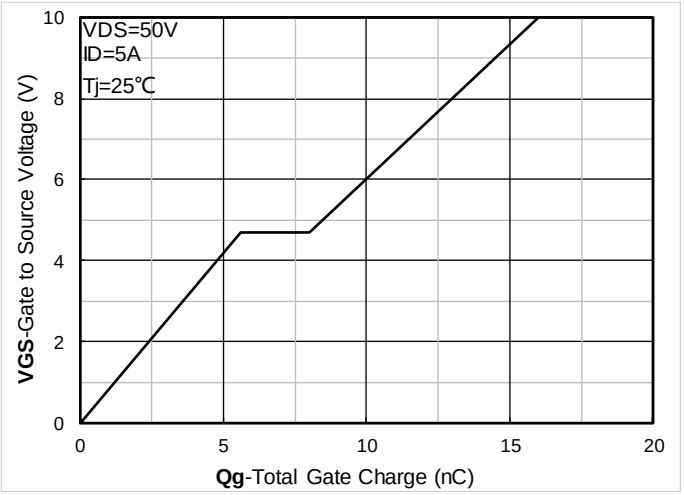


Figure 4. Gate Charge

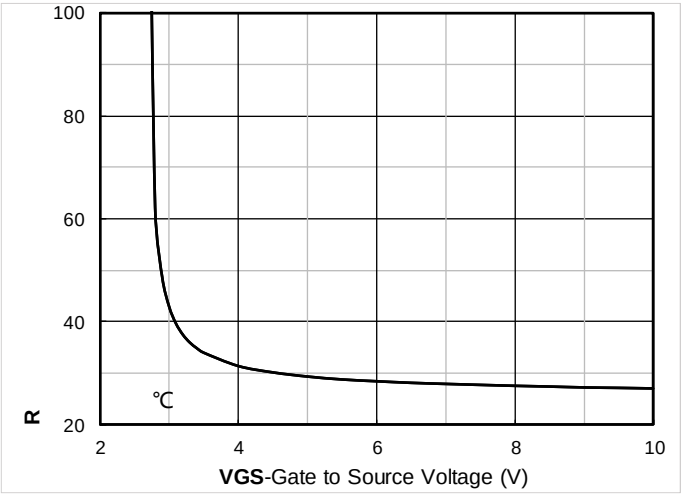


Figure 5. On-Resistance vs Gate to Source Voltage

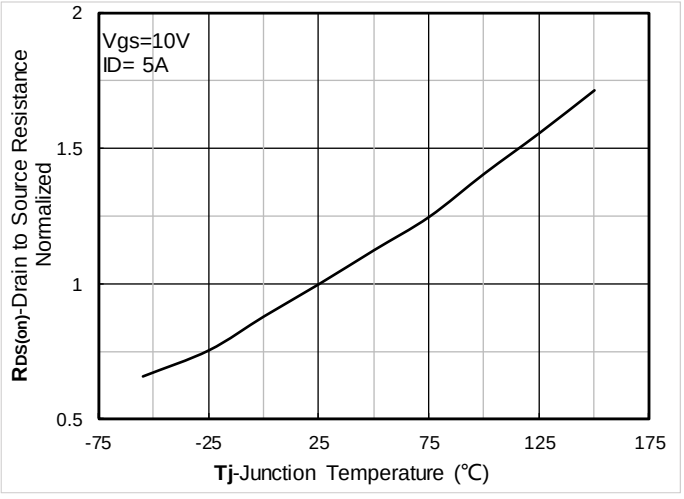


Figure 6. Normalized On-Resistan

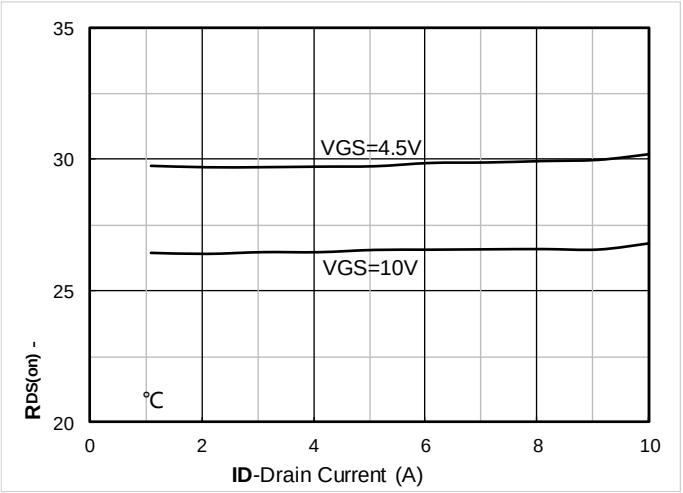


Figure 7. $R_{DS(on)}$ VS Drain Current

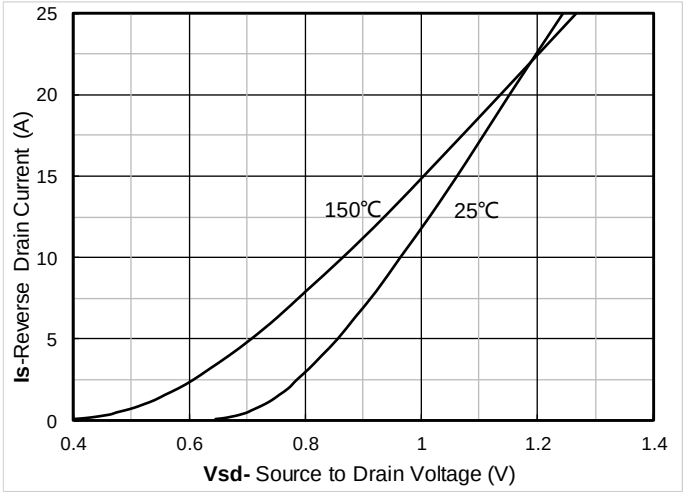


Figure 8. Forward characteristics of reverse diode

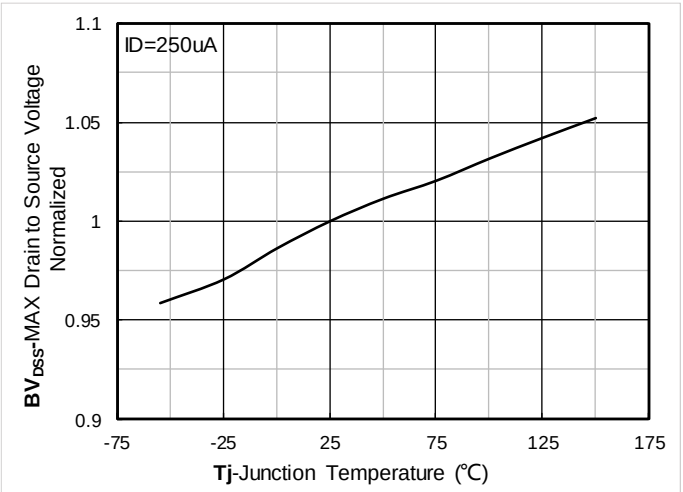


Figure 9. Normalized breakdown voltage

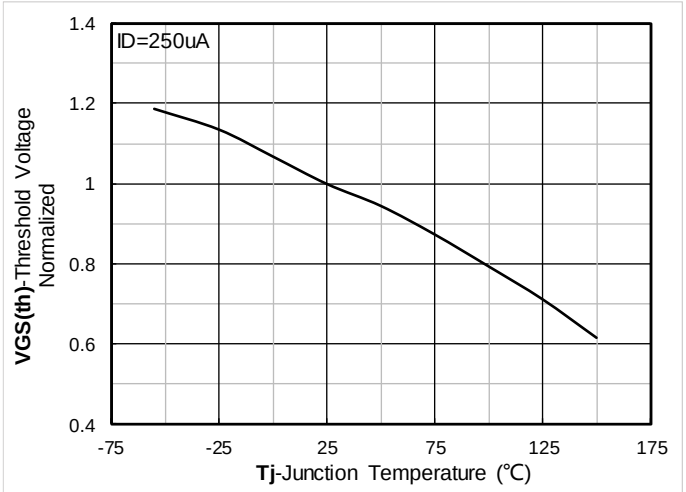


Figure 10. Normalized Threshold voltage

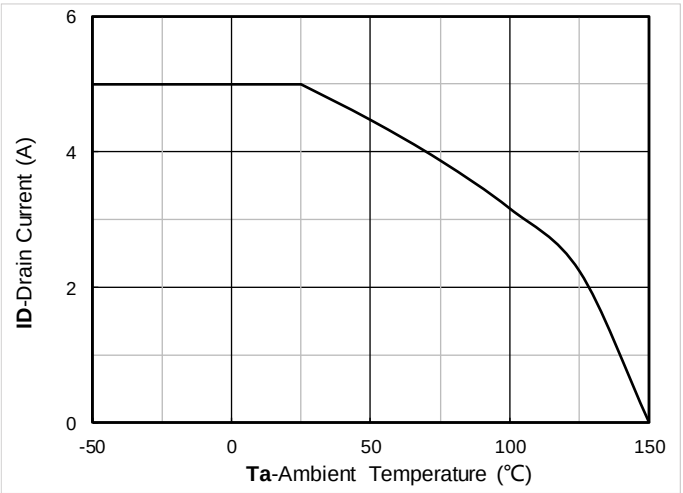


Figure 11. Current dissipation

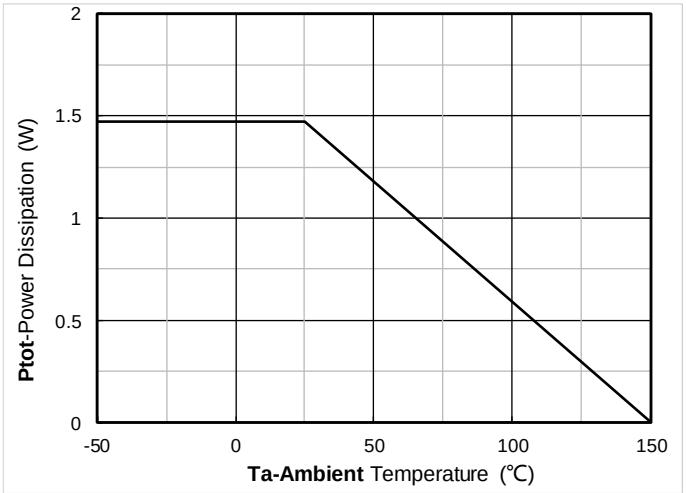


Figure 12. Power dissipation

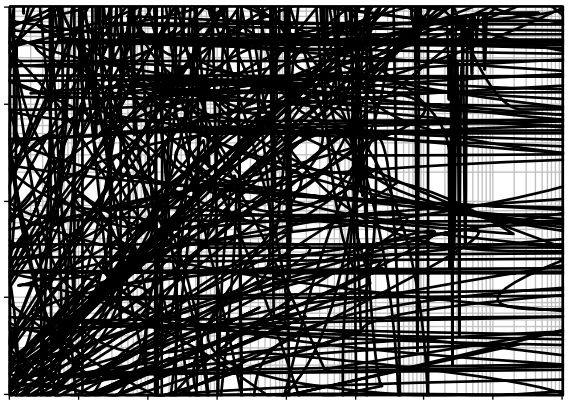


Figure 13. Maximum Transient Thermal Impedance

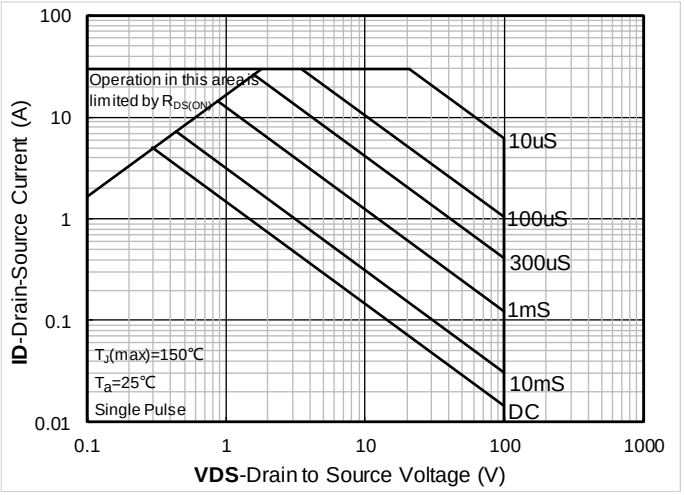


Figure 14. Safe Operation Area

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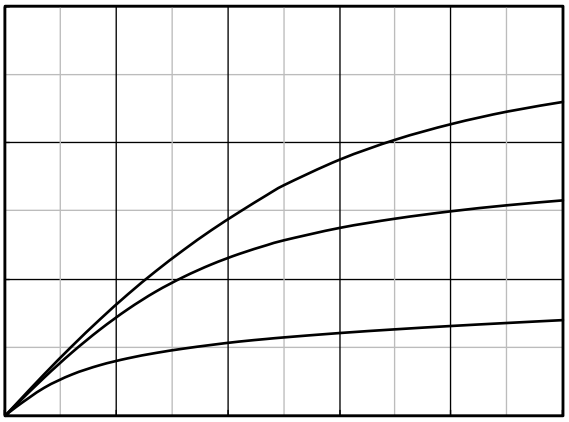


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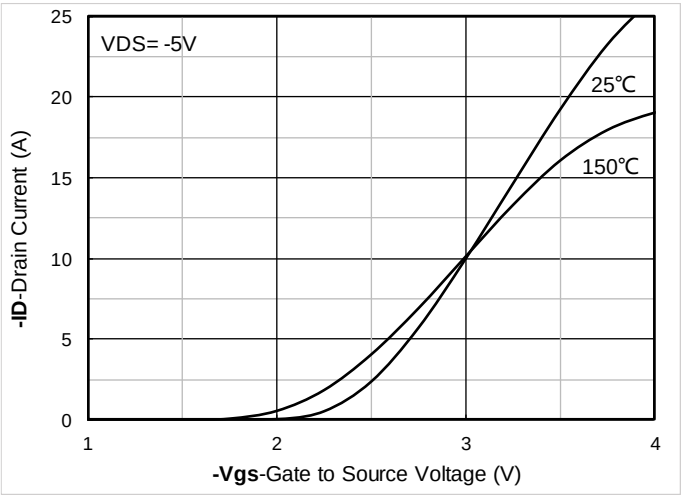


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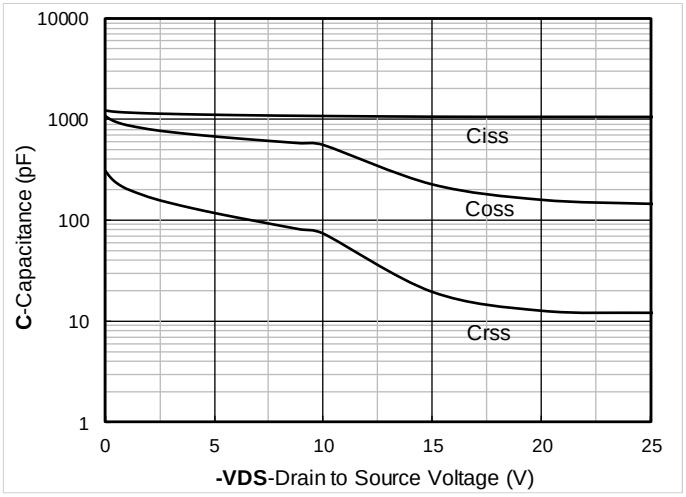


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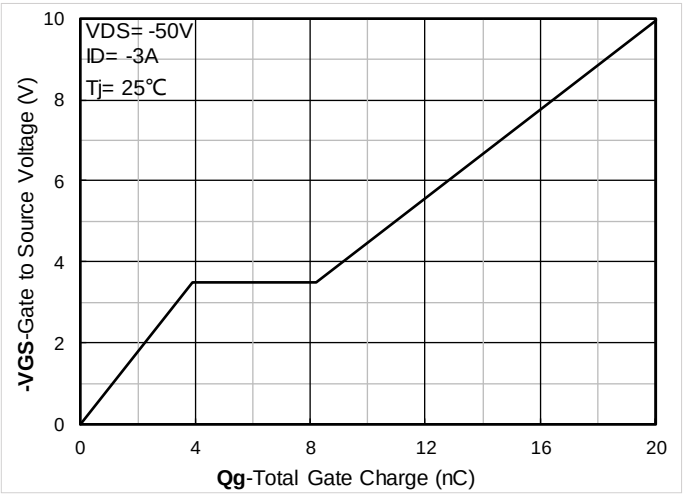


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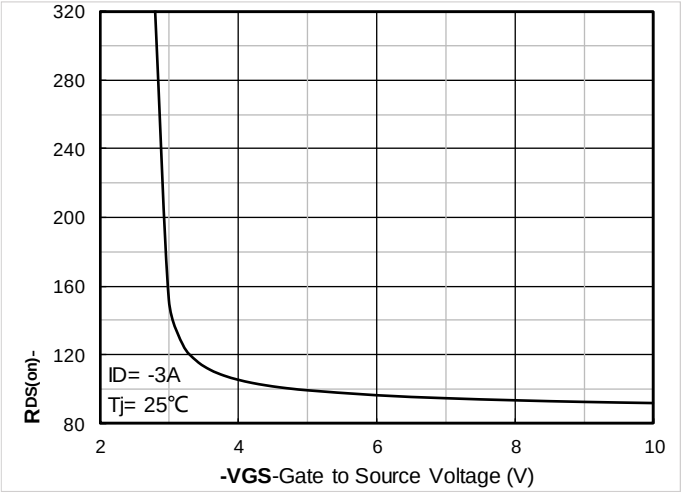


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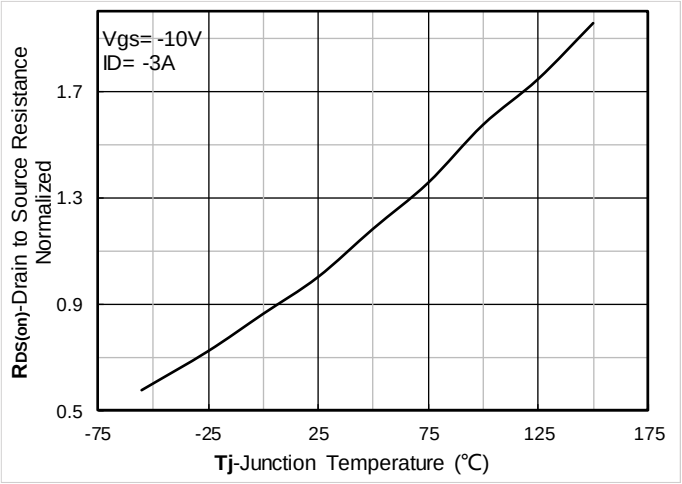


Figure 6. Normalized On-Resistance

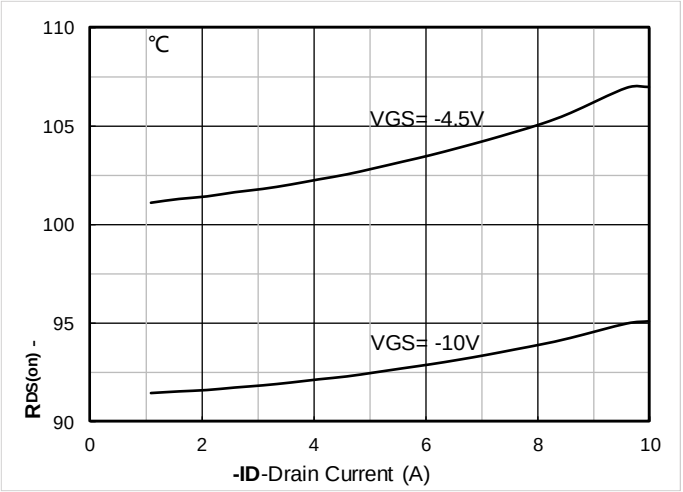


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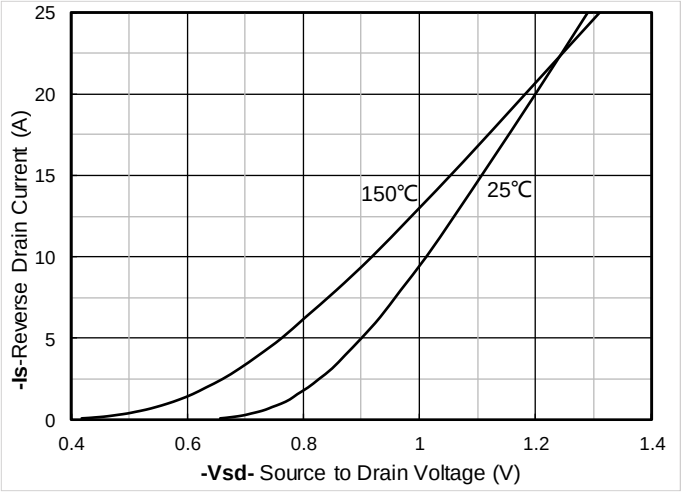


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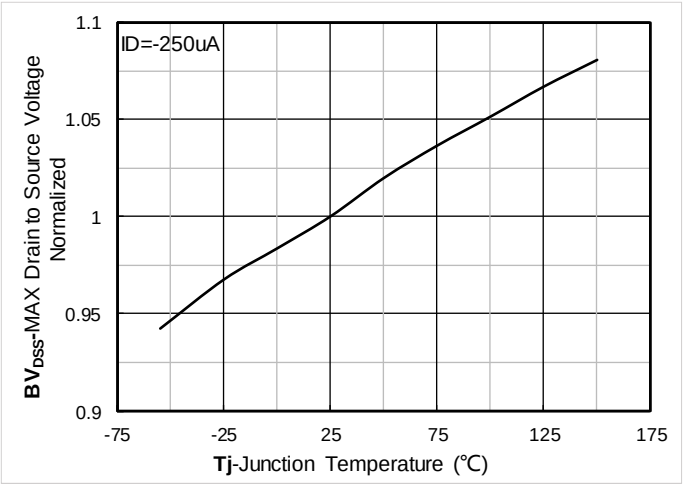


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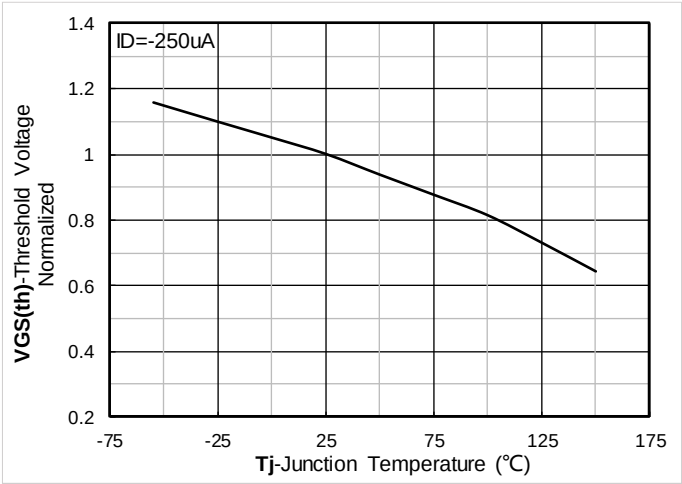


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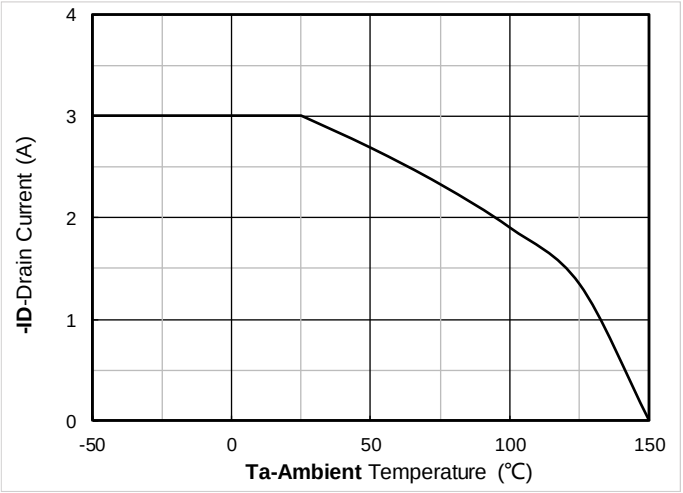


Figure 11. Current dissipation

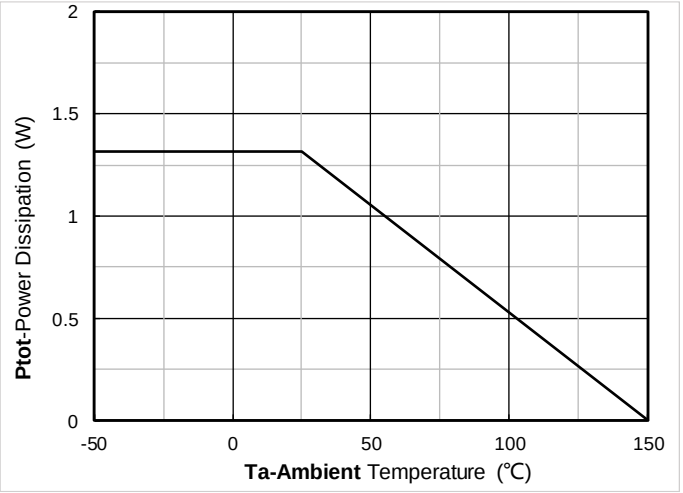


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Figure 13. Maximum Transient Thermal Impedance

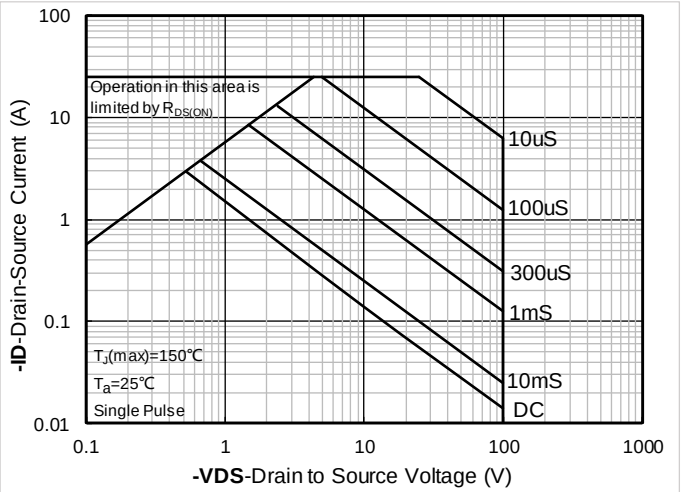


Figure 14. Safe Operation Area

SOP-8 Package information

SYMBOL	MIN.		
	0		
B			
D		0.020	
E			
F			
	0.050BSC		
H J			
K			

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