N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	100V
I_D	15A
$R_{DS(ON)}$(at V_{GS}=10V)	9.5 mohm
100% EAS Tested	

General Description

Split Gate Trench MOSFET technology
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$

Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

DC/DC Primary Side Switch
Telecom/Server
Synchronous Rectification

Absolute Maximum Ratings (T_A=25 unless o

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V, T_J=25			1	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ± 20V, V_{DS}=0V			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250	2.0	2.8	4.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=10A		8.0	9.5	
Diode Forward Voltage	V_{SD}	I_S=15A,V_{GS}=0V			1.3	V
Maximum Body-Diode Continuous Current	I_S				15	A
Gate resistance	R_G	f=1MHz, Open drain		0.68		
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHZ		2270		pF
Output Capacitance	C_{oss}			797		
Reverse Transfer Capacitance	C_{rss}			36		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=10A		32		nC
Gate-Source Charge	Q_{gs}			11.1		
Gate-Drain Charge	Q_{gd}			4.78		
Reverse Recovery Chrage	Q_{rr}	I_F=10A, di/dt=100A/us		84		nC
Reverse Recovery Time	t_{rr}			51.5		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=50V,I_D=10A R_{GEN}=2.2		51		ns
Turn-on Rise Time	t_r			14.4		
Turn-off Delay Time	$t_{D(off)}$			69.2		
Turn-off fall Time	t_f			20.6		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. Pd is based on max. junction temperature, using ≤10s junction-ambient thermal resistance.

C. The value of R_{JA} is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

Typical Performance Characteristics

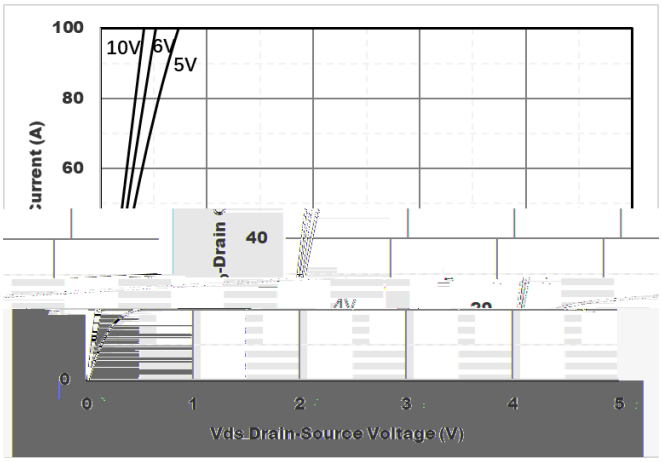


Figure1. Output Characteristics

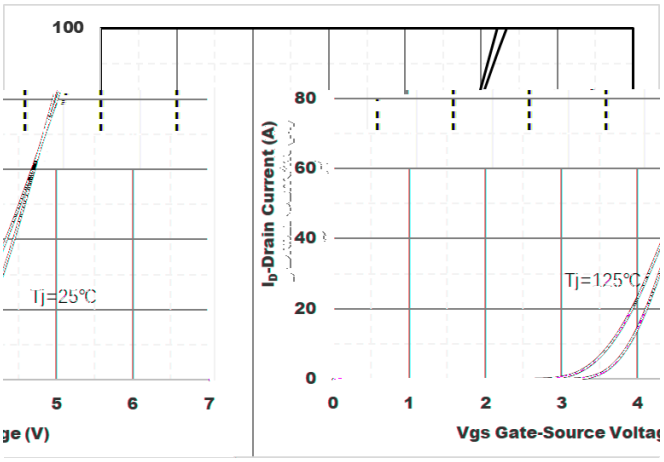


Figure2. Transfer Characteristics

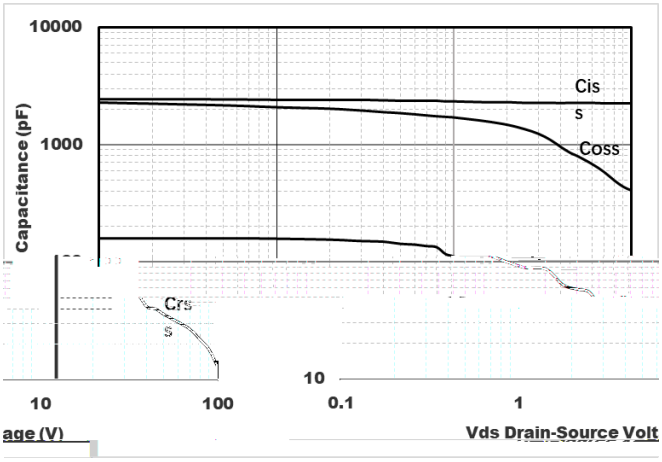


Figure3. Capacitance Characteristics

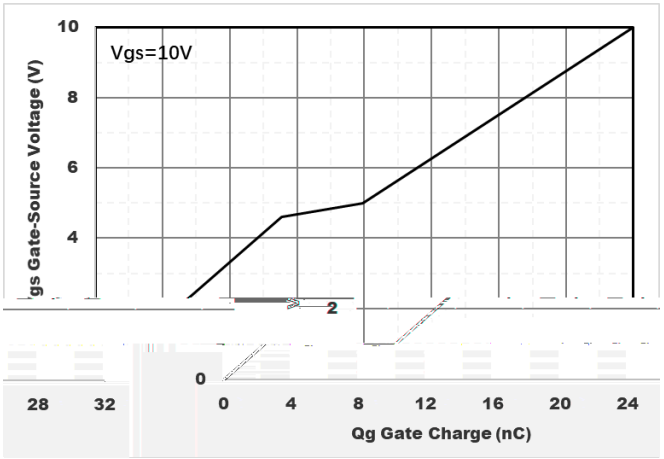


Figure4. Gate Charge

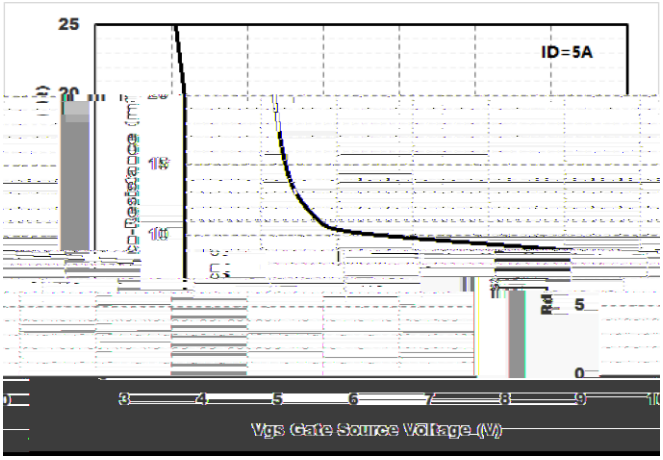


Figure5. Drain-Source on Resistance

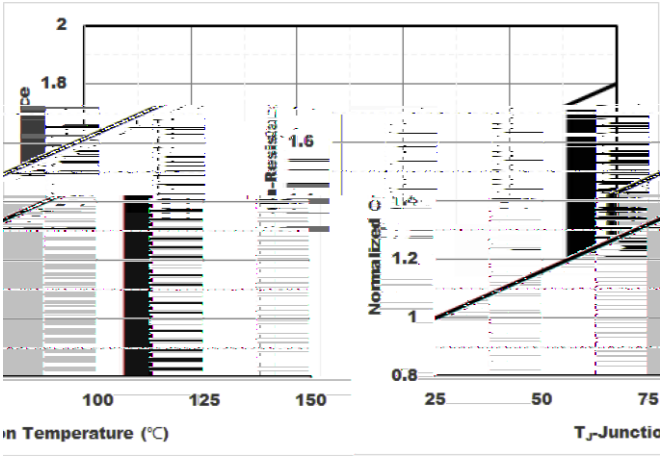


Figure6. Drain Current

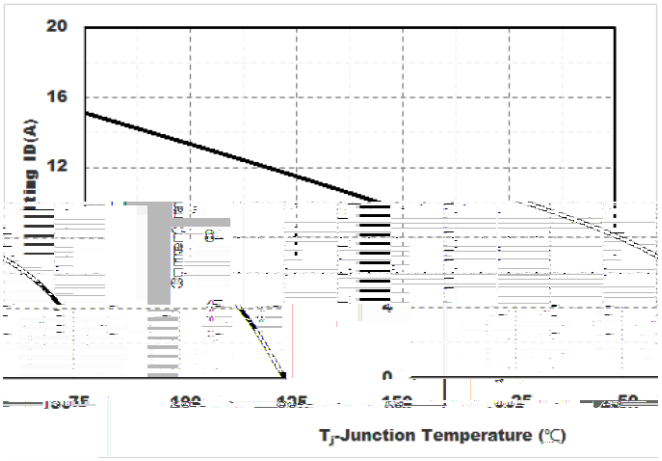


Figure7. Drain current

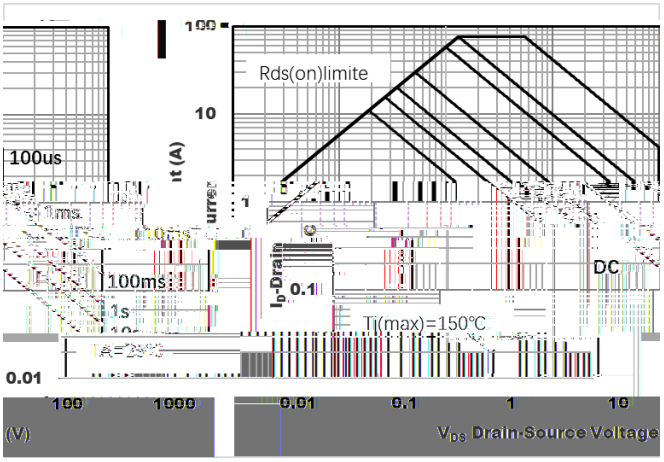


Figure8. Safe Operation Area

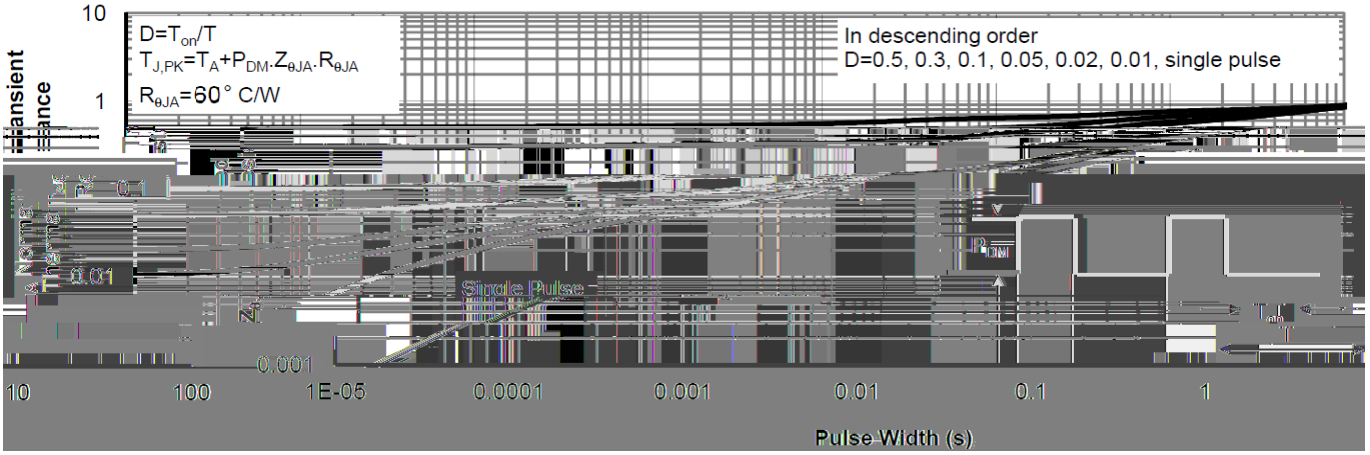
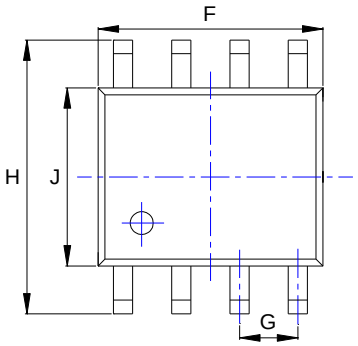
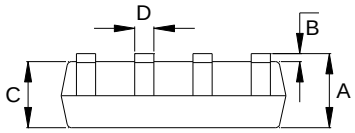


Figure9. Normalized Maximum Transient Thermal Impedance

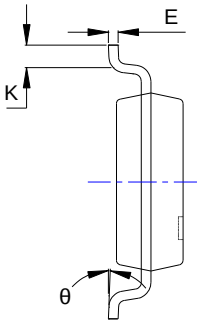
SOP-8 Package information



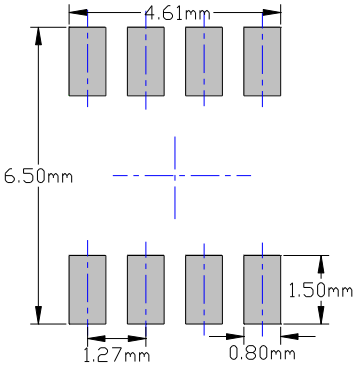
TOP VIEW



SIDE VIEW



SIDE VIEW



Suggested Solder Pad Layout

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.05mm.
3.The pad layout is for reference purposes only.

Disclaimer